Application Bulletin AB-15

Using Surface Mount Power MOSFETs in Processor Power Supplies

Summary

Surface mount power MOSFETs are becoming increasingly popular for use in processors' switch-mode power supplies. Ensuring that they operate as planned requires careful attention to their thermal environment, in particular pad size. This Application Bulletin gives the designer and the layout specialist the information necessary to create a successful design.

Introduction

The price of surface mount power MOSFETs has steadily dropped over the years, to the point where now they are essentially the same price as TO-220s (for the same die). When account is taken of heatsinking costs of the TO-220 package—the heatsink itself, possibly a screw, labor—the surface mount part may actually turn out to be cheaper. For this reason, using surface mount power MOSFETs for processors' switch-mode power supplies will become increasingly the first choice for motherboards.

Just as design with the TO-220 package required careful attention to the sizing of a heatsink to control the MOSFETs' thermal environment, there are a new set of potential problems with the surface mount power packages relating to heat removal. There are not many options for attaching a heatsink to a surface mount power package, and so the primary method of removing heat is through the pads.

For packages such as the SO-8, the only available pads are those for the pins, making power dissipation very limited. There is one surface mount power package, however, the TO-263 (D^2PAK), which has a large pad: much of the back side of the package, which is the drain, is metallic. A large pad can be used here, enhancing not only the thermal characteristics, but also serving as a power connection. For this reason, this Application Bulletin concentrates on proper heatsinking using the D^2PAK.

Thermal Basics

The goal of thermal control is to prevent the MOSFET from becoming so hot that it self-destructs—or more optimistically, so that it can achieve the desired lifetime of the converter. When the MOSFET dissipates a certain amount of power, this power actually heats the die inside the package. The heat then travels through the package to the pads, and the pads conduct it away.

There is an exact analogy between this process and an electrical network. Just as an electrical network has resistors and capacitors, there are thermal resistances and thermal capacitances. (This Application Bulletin doesn't consider thermal capacitance.) Thermal resistances in series add, etc. Consider Figure 1, which shows on the left a MOSFET dissipating 2W; it has a thermal resistance to the ambient (Θ_{JA}) of 30°C/W, and the ambient temperature is 40°C. Corresponding to the 2W power source on the left is a 2A current source shown on the right. Corresponding to the thermal resistance of 30°C/W is a resistor of 30Ω; and corresponding to the ambient temperature of 40°C is a battery of 40V. The picture below makes it clear that the current source sees 100V; correspondingly, then, the MOSFET on the left sees 100°C.

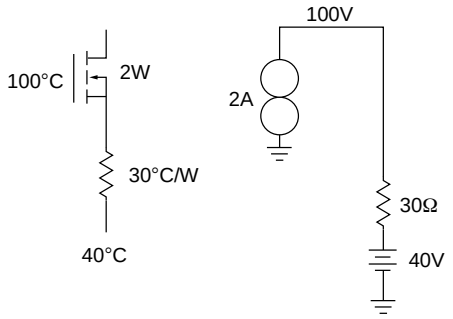

Figure 1. There is an Exact Analogy Between Power Dissipation and Thermal Resistance (on the Left) and Current Sources and Resistance (on the Right). Voltage on the Right Corresponds to Temperature on the Left.

Thermal Characteristics

Θ_{JA}, the power dissipation, and the ambient temperature thus determine the MOSFET's junction temperature. Given a certain power dissipation in the MOSFET, the pad must be sized to provide a suitable Θ_{JA}. Fairchild Semiconductor has conducted experimental tests to determine pad size (see Figure 2).

D²PAK (TO-263) Power MOSFET Typical Thermal Data

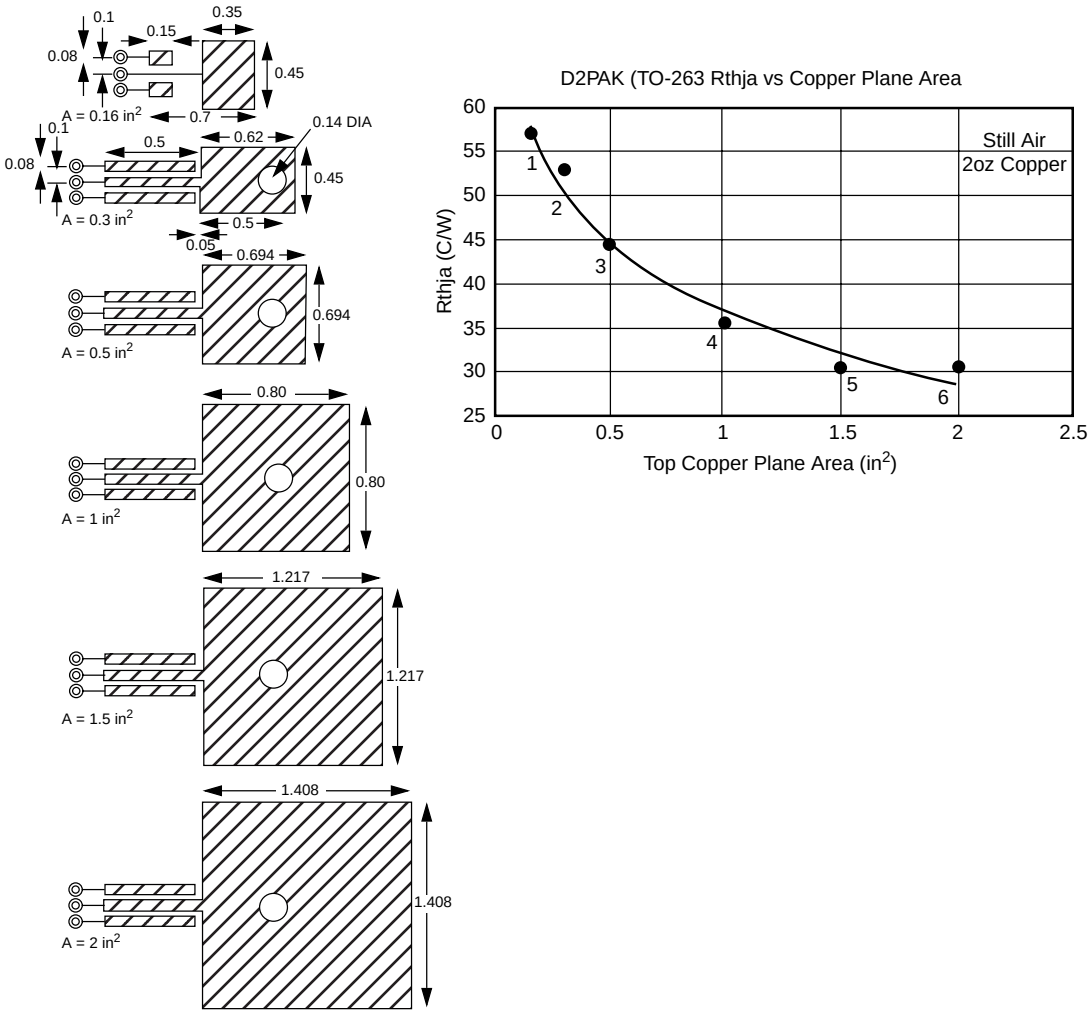

Figure 2. D²PAK Thermal Data (Courtesy of Alan Li, Fairchild Semiconductor Discrete Power and Signal Technologies)

The chart in Figure 2 may be used as follows.

$$\text{Required } \Theta_{JA} = \frac{T_{die} - T_{ambient}}{P_{dissipated}}$$

Thus, as in the previous example, suppose that the ambient is 40°C, the die is allowed to reach only 100°C, and the power dissipated is 2W. Then the required Θ_{JA} is

$$\Theta_{JA} = \frac{100°C - 40°C}{2W} = 30°C/W$$

consistent with the results of Figure 1. To achieve 30°C/W, we read off the chart that a pad size of approximately 1.75in^2 is required. As an alternative, the curve shown in Figure 2 may be approximated by the equation

$$\Theta_{JA} = 35A^{-0.274}$$

The embedded Excel spreadsheet shown as Figure 3 calculates the pad area from the parameters automatically: just enter the parameters and the required pad area is calculated.

Maximum MOSFET Temperature	100	C
Ambient Temperature	40	C
MOSFET Power Dissipation	2	W
Pad Area Required	1.8	Square inches

Figure 3. This is an Embedded Excel Spreadsheet for Calculating the Required Pad Size of a D^{2}PAK MOSFET.

Reducing the Pad Size

1.8in^2 is a very large pad. If a better MOSFET were used, this would reduce the power loss and thus the required pad size. However, there may be economic or availability reasons why this is not practical. A better alternative may be to use two MOSFETs in parallel rather than one. (Refer to Application Bulletin AB-9 for some electrical information on paralleling MOSFETs.) Not only does this reduce the net on-resistance, lowering the total power dissipated, but it also distributes the power losses amongst two packages. This thus very substantially reduces pad size.

For the example calculation, suppose that two MOSFETs are used instead of one. Total on-resistance has been cut in half, but switching losses are slightly increased because of increased gate capacitance for the IC gate drive. Total power dissipation is reduced, let's say to 1.4W. This 1.4W is distributed between two packages, and so each package dissipates only 0.7W. Using the spreadsheet in Figure 3, we find that the pad size for each MOSFET is now only 0.04in^2! This is smaller than the package outline, and so instead of a single pad of 1.8in^2, we have two pads of 0.16in^2 each (minimum pad size for the D^{2}PAK), for a substantially reduced total area.

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